REMARKS

Claims 1-30 remain pending with claims 1, 11, 20, and 25 being independent.

The remainder of the remarks follow a copy of the Office Action text:

> Claims 1-6, 9-15 and 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow et al. (US 6,148,349) in view of Matsunami et al. (US 6,542,961).
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> 4. Regarding claim 1, 6, 9-11, 15 and 18-20, Chow discloses a system module (fig. 2, item 226) to couple a switch fabric network (item 106) to shared I/O resources (items 224). The module comprises a first serverlet (figs. 2 and 3, item 212) and a second serverlet (figs. 2 and 3, item 214). As presented in the claim amendment, the system also comprises a second switching device (fig. 8, item 802; col. 25, lines 44-50) to couple to the switch fabric network and the first and second serverlets. However, Chow does not disclose a switch and bus for coupling the serverlets to the I/O resources. Matsunami discloses processors (fig. 1, item 30) coupled to I/O resources (item 10; fig. 2) by a switch (item 20; fig. 3) and a data bus (items 31). The switch has a controller device (item 70), a switching device to couple the first interface device to the second interface device (fig. 1, item 20; note: port connections from each host to the switch), and has a third interface device (fig. 1, item 204) to couple between the second switching device and another data bus (item 21). The data bus (item 21) is coupled to the I/O resources and the controller couples the inherent second switching device to the data bus. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have a switch and bus couple serverlets to I/O resources in the invention of Chow in order to enhance scalability or improve reliability (Matsunami, col. 12, lines 4-14 and 40).

Applicant disagrees with the analysis above in several regards.

First, Applicant disagrees that it would have been obvious to modify Chow with the switches of Matsunami as proposed above. In Chow, hosts 102 attach to the BYNET Interconnect fabric 106. In Matsunami, hosts 30 attach to the diskarray switches 20. A logical combination of Chow and Matsunami would replace the BYNET Interconnect fabric 106 of Chow with the diskarray switches 20 of Matsunami. However, such a combination would not yield the claimed subject matter of claim 1. While the Applicants understand that the Examiner proposed interposing the diskarray switches between the ION's 212, 214 and the JBODs 222, 218 and not replacing the BYNET fabric, Applicants believe the proposed combination does not reflect the described function of the diskarray switches 20. Additionally, even if the proposed combination were constructed, the insertion of the diskarrary switches between the IONs and the JBODs 222, 218 would create a bottleneck in JBOD access by the ION's 212, 214 (e.g., only a single ION could have access to JBODs 222, 218 at a time). This is contrary to the dual ION operation described in Chow.

Secondly, Applicant disagrees that Chow describes a switch device to couple serverlets to a switch fabric. Chow describes an interface 802 (see FIG. 8) to the BYNET fabric provided by a processor that executes programs to DMA (Direct Memory Access) "PIT" (Put-it-there) packets to/from ION 212 memory (see col. 25, lines 38-50 and the section entitled "PIT Protocol In Action - Disk, Read and Write" starting at column 29, line 24). Applicants disagree that a processor executing DMA programs comprises a switching device to couple serverlets to a switch fabric. Thus, even if one of skill in the art would combine Chow and Matsunami in the proposed fashion, due to the absence of a switching device coupling the serverlets to a switch fabric, the resulting combination would still not provide the subject matter recited by claim 1.

Claims 11 and 20 recite a similar limitation. Applicants respectfully request withdrawal of the reject of claims 1, 11, and 20 and their dependent claims.

10. Regarding claims 25-26 and 29, Chow discloses a system (fig. 2) comprising several serverlets (items 212 and 214) each comprising a processor and memory (fig. 3, item 304) and a power conversion unit (item 306). The serverlets are coupled to a shared disk system (fig. 2, item 218 and 222) and a switch fabric network (106). However, Chow does not disclose that the serverlets include a DIMM and that the system includes a chassis comprising first and second switching devices. Hipp discloses a system (fig. 1, item 38) comprising serverlets (item 32; fig. 2) comprising a DIMM (fig. 2, item 93; col. 10, lines 37-43), and a chassis (item 38) to house multiple serverlets. The chassis comprises a first switching device (fig. 1, item 48; fig. 5; col. 12, lines 47-50 and 62-65) to couple a shared disk system (fig. 1, item 54) and a second switching device (fig. 1, item 40; col. 12, lines 37-40 and 47-50) to couple to a switched fabric network (item 45). The system includes a data bus (fig. 1, item 34) to connect the serverlets to the switching devices, where the first and second data buses are the same. The serverlets of the system (fig 10, item 32) do not include a cooling system (fig. 10, item 264-269). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have a server chassis for serverlets of the invention of Chow in order to simplify or make easier the implementation of several computing resources.

As amended, claim 25 recites a switching device that couples the serverlets to the disk system(s) via a bus connecting the switching device and the disk systems. For example, the specification describes a SCSI or PCI backplane bus/interface coupling the switching device and the disk systems. Hipp does not describe or suggest such a coupling. Thus, assuming that one would combine the very different functional aspects of Hipp and Chow, the resulting combination would still not provide the recited subject matter.

Applicants respectfully request withdrawal of the rejection of claim 25 and its dependent claims.

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